Life in the FAST lane

TechSAT has developed a new test system architecture, called FAST (future architecture system testing), which simplifies test installations for safety-critical applications found in modern aerospace and avionics industry.

FAST is an I/O subsystem that can be integrated in any test system via Fast Ethernet. The concept comprises a family of self-contained modules designed for processing standard and avionics-specific signals as well as for simulation, monitoring, and routing between UUT, original equipment, and test system.

Rigorous admission regulations for safety-critical systems demand clear and precise specifications of system requirements, modes of behavior, failure rates, and reliability values. To this end, manufacturers must prove the fulfillment of these requirements, demonstrate the correct implementation of the functionality by prototypes, and finally validate their implementation through incremental test stages including board test, system integration, and functional integration.

Current simulation environments and test systems keep adding more and more complexity, thereby inflating the 'cost of test'.

With FAST, TechSAT has developed a concept that, based on a compact architecture, both increases the reliability of test systems and, at the same time, reduces their costs significantly. To reach this goal, TechSAT loosened the strict separation of hardware functions and, instead, integrated the essential functions into the FAST modules in a signal-specific way. As an example, for Hardware-in-the-Loop (HiL) testing, FAST provides an interface to the original equipment (OE) for typical signal processing applications, such as reading, writing, analysis, and fault stimulation, including stress and limit tests.

A FAST module can be used in simulation mode and, alternatively, as a monitor between the OE and up to two units or systems under test (UUT/SUT). The model behavior can be directly compared to the tested equipment, permitting quick diagnostics of potential faults. A FAST system can consist of individual modules, a subsystem crate with 21 module slots, or a logical subsystem combining several modules or crates.

This flexibility is achieved through the following core features: standardized interfaces for signal transmission, programmable signal conditioning and stimulation/error injection, hardware and logical scalability, API for integrating test applications, and full integration into TechSAT's Avionics Development System ADS2.

With an uncomplicated connection via Ethernet, the configuration of modules and subsystems is very adaptable and inexpensive. Moreover, errors in the system configuration can be analyzed and fixed quickly and easily. Since a considerable amount of test system wiring can be saved, the FAST concept also decreases the overall development costs of the entire test system.

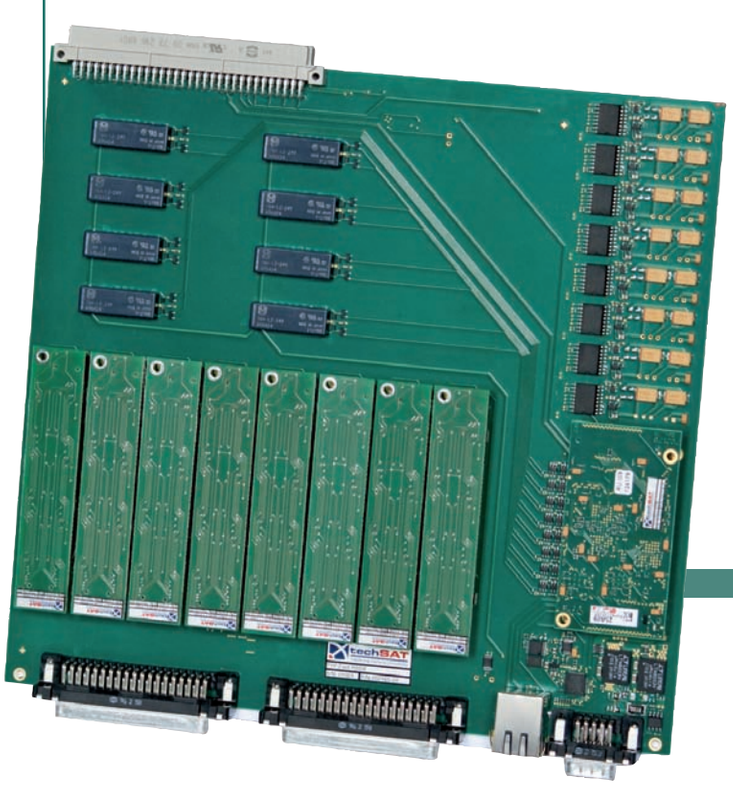
Each FAST family member has a local CPU running an embedded Linux OS. The CPU is released from time-critical I/O tasks by either an FPGA or DSP core computing the I/O without interaction of the main CPU. Time-stamping of all activities allows for distinct analysis of cause and action within complex, multidomain test systems.

The FAST subsystem can be operated in either of two modes, frame-based or event-driven. Events can be generated through predefined conditions, such as signal limits or signal filters, or through programs executing locally on the FAST module. Due to the open source Linux OS, extensive development support is provided to write these programs.

Synchronization of all FAST modules within a subsystem is accomplished by a time sync bus, such as IRIG-B, GPS, or NTP.

With the avionics industry in mind, FAST supports customized test scenarios with various I/Os, such as analog, digital, and proprietary serial interfaces as well as resistive sensor simulation and current loads. The integration into the test system is achieved through a uniform software API interface.

A FAST module incorporates the following functions: host communication via standardized LAN, built-in microcontroller for gathering the signals of the entire system and translating internal control commands, signal processing through integrated FPGA or DSP, signal conditioning, digital I/O, analog I/O, programmable simulation of pressure and temperature sensors, stimulation and injection of programmable failures directly on the FAST module, internal switching between original equipment and simulated components, and time synchronization via optional Timemaster (NTP, IRIG-B, etc).



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